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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/649,833	08/28/2003	Kazuhiro Nakajima	NE-1144-US/kwg	7153

21254 7590 03/09/2005

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EXAMINER	
SHINGLETON, MICHAEL B	
ART UNIT	PAPER NUMBER
2817	

DATE MAILED: 03/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)
	10/649,833	NAKAJIMA, KAZUHIRO
	Examiner	**Art Unit**
	Michael B. Shingleton	2817

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ~~4~~ Three MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-30 ~~is~~/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) 23-30 ~~is~~/are allowed.

6)☒ Claim(s) 1-22 ~~is~~/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 8/28/03, 4/28/04

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

Specification

The disclosure is objected to because of the following informalities: On page 9 line 31 it appears that "transfer gates 20" was meant instead of "transfer gates 18". On page 13, lines 5 and 6 it appears that "MOSFETs 22 and 24 of the ring oscillator 10" was meant instead of "MOSFETs 22 and 24 of he ring oscillator 10".

Appropriate correction is required.

The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: Claims like claim 1 recites a "positive feedback loop" that includes a plurality of delaying stages connected in cascade. However, the specification recites the "positive feedback loop" as just line "16" or "16A" that does not include a plurality of delaying stages. It appears that there is merely confusion with the terminology used and not the issue of the claims setting forth an invention not described in the specification, thus the rejection based on art will be on what the examiner believes the claim structure corresponds to in the specification even though the claim terminology does not correspond the same claim terminology of the specification.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2 and 21 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by IBM Technical Disclosure Bulletin vol. 33 No. 10A March 1991 (IBM).

Figure 1 and the relevant text of IBM discloses a voltage controller oscillator that has as part of its internal structure a ring oscillator composed of a feedback input terminal (The node that is directly connected to transistors Q13 and Q14 and line marked "OSCO".). Note that applicant calls the line 16 the positive feedback loop in the specification and thus the "line", i.e. conductors connected between the two transistors Q13 and Q14, and the line marked "OSCO" forms the same "positive feedback loop" as per the specification. Also note the discussion below concerning the terminology "positive feedback loop" as per the plurality of delay stages. IBM also discloses a circuit output terminal "OSCO" that is clearly for generating an oscillator output signal and a "positive feedback loop" that is composed of a plurality of delay stages, i.e. like transistors Q2, Q7 and Q11 connected in cascade, and a transfer gate coupled to

each of the plurality of delay stages. The transfer gates are composed of transistors like (Q5, Q6), (Q9, Q10), (Q13, Q14) wherein each of these transfer gates are composed of a pair of complementary transistors connected in parallel. The transfer gate transistors of the first conductivity type being controlled by a first control signal "PDEV" and the transfer gate transistors of the second conductivity type being controlled by a second control signal "NDEV". There are an odd number of delaying inverter stages like (Q7 and Q8) and (Q2 and Q3) clearly shown by IBM. These inverter stages are CMOS as is clearly illustrated in IBM. The claims recite the functional language "wherein said ring oscillator is operable during a first mode when said p-channel transistors are ON and said n-channel transistors are OFF, during a second mode when said p-channel transistors are OFF and said n-channel transistors are ON, and during a third mode when said p-channel and n-channel transistors are both ON". IBM recognizes that by changing the voltage of the two control signals that control the transfer gates that the time constant can be changed. Because the claim(s) do not recite a control signal source, the IBM reference has all of the claimed structure. Also the ring oscillator structure itself is clearly capable of providing for the functional language as recited above. This still results in the changing of the time constants as recognized by IBM. Thus IBM is fully capable of performing the recited function, (See MPEP 2114). Note that IBM clearly illustrates that each of the transfer gates is coupled to the input of one of the CMOS inverters that follow the transfer gate. Note that Q1 and Q4 forms part of an enable sircuit fo the oscillator. When "IN" is "low" the oscillator will oscillate i.e. Q2 and Q3 will form an inverter delay element. (See page 288 of IBM.)

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3, 5 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over IBM Technical Disclosure Bulletin vol. 33 No. 10A March 1991 (IBM) in view of Taito et al. 6,781,431 (Taito).

Figure 1 and the relevant text of IBM discloses a voltage controller oscillator that has as part of its internal structure a ring oscillator composed of a feedback input terminal (The node that is directly

connected to transistors Q13 and Q14 and line marked "OSCO".). Note that applicant calls the line 16 the positive feedback loop in the specification and thus the "line", i.e. conductors connected between the two transistors Q13 and Q14, and the line marked "OSCO" forms the same "positive feedback loop" as per the specification. Also note the discussion below concerning the terminology "positive feedback loop" as per the plurality of delay stages. IBM also discloses a circuit output terminal "OSCO" that is clearly for generating an oscillator output signal and a "positive feedback loop" that is composed of a plurality of delay stages, i.e. like transistors Q2, Q7 and Q11 connected in cascade, and a transfer gate coupled to each of the plurality of delay stages. The transfer gates are composed of transistors like (Q5, Q6), (Q9, Q10), (Q13, Q14) wherein each of these transfer gates are composed of a pair of complementary transistors connected in parallel. The transfer gate transistors of the first conductivity type being controlled by a first control signal "PDEV" and the transfer gate transistors of the second conductivity type being controlled by a second control signal "NDEV". There are an odd number of delaying inverter stages like (Q7 and Q8) and (Q2 and Q3) clearly shown by IBM. These inverter stages are CMOS as is clearly illustrated in IBM. The claims recite the functional language "wherein said ring oscillator is operable during a first mode when said p-channel transistors are ON and said n-channel transistors are OFF, during a second mode when said p-channel transistors are OFF and said n-channel transistors are ON, and during a third mode when said p-channel and n-channel transistors are both ON". IBM recognizes that by changing the voltage of the two control signals that control the transfer gates that the time constant can be changed. Because the claim(s) do not recite a control signal source, the IBM reference has all of the claimed structure. Also the ring oscillator structure itself is clearly capable of providing for the functional language as recited above. This still results in the changing of the time constants as recognized by IBM. Thus IBM is fully capable of performing the recited function, (See MPEP 2114). Note that IBM clearly illustrates that each of the transfer gates is coupled to the input of one of the CMOS inverters that follow the transfer gate. Note that Q1 and Q4 forms part of an enable sircuit fo the oscillator. When "IN" is "low" the oscillator will oscillate i.e. Q2 and Q3 will form an inverter delay element. (See page 288 of IBM.) IBM is silent on showing of the structure that produces the two control signals that control the transfer gate transistors. Claim 5 recites that the first and second control signals both have two levels. Clearly these control signals of IBM each have at least two levels which is all that is required by the claim language. Claim 5 also sets forth that the claimed invention further includes "a control circuit in communication with [the] gates of said p-channel transistors with [the] gate of said n-channel transistors for shifting said first control signal between said two levels thereof and said second control signal between said two levels thereof". There must be a control circuit to provide the

multiple control signal levels in IBM. IBM is merely silent on the details of such a circuit. Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have utilized a control circuit that can switch between the at least two levels of the first and second control signals in IBM because, as the IBM reference is silent on the exact control circuit used one of ordinary skill in the art would have been motivated to use any art-recognized equivalent control circuit such as the conventional control circuit that provides at least two signal levels for each of the control signals. IBM is silent on the use of a NAND gate in place of one of the delay elements.

Figure 12 of Taito discloses the use of a NAND gate use in place of one of the delay elements in a ring oscillator so as to add the function of enablement/disablement and that this is an art recognized equivalent way to enable or disable a ring oscillator.

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to have replace on the delay/or element (Q1-Q4) of IBM with a NAND gate given that the NAND structure of Taito is an art recognized equivalent way to enable or disable a ring oscillator as compared to other conventional enable/disable circuits and so as to allow for an enable signal to control the enablement of the ring oscillator as taught by Taito.

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over IBM Technical Disclosure Bulletin vol. 33 No. 10A March 1991 (IBM).

Figure 1 and the relevant text of IBM discloses a voltage controller oscillator that has as part of its internal structure a ring oscillator composed of a feedback input terminal (The node that is directly connected to transistors Q13 and Q14 and line marked "OSCO".). Note that applicant calls the line 16 the positive feedback loop in the specification and thus the "line", i.e. conductors connected between the two transistors Q13 and Q14, and the line marked "OSCO" forms the same "positive feedback loop" as per the specification. Also note the discussion below concerning the terminology "positive feedback loop" as per the plurality of delay stages. IBM also discloses a circuit output terminal "OSCO" that is clearly for generating an oscillator output signal and a "positive feedback loop" that is composed of a plurality of delay stages, i.e. like transistors Q2, Q7 and Q11 connected in cascade, and a transfer gate coupled to each of the plurality of delay stages. The transfer gates are composed of transistors like (Q5, Q6), (Q9, Q10), (Q13, Q14) wherein each of these transfer gates are composed of a pair of complementary transistors connected in parallel. The transfer gate transistors of the first conductivity type being controlled by a first control signal "PDEV" and the transfer gate transistors of the second conductivity type being controlled by a second control signal "NDEV". There are an odd number of delaying inverter

stages like (Q7 and Q8) and (Q2 and Q3) clearly shown by IBM. These inverter stages are CMOS as is clearly illustrated in IBM. The claims recite the functional language "wherein said ring oscillator is operable during a first mode when said p-channel transistors are ON and said n-channel transistors are OFF, during a second mode when said p-channel transistors are OFF and said n-channel transistors are ON, and during a third mode when said p-channel and n-channel transistors are both ON". IBM recognizes that by changing the voltage of the two control signals that control the transfer gates that the time constant can be changed. Because the claim(s) do not recite a control signal source, the IBM reference has all of the claimed structure. Also the ring oscillator structure itself is clearly capable of providing for the functional language as recited above. This still results in the changing of the time constants as recognized by IBM. Thus IBM is fully capable of performing the recited function, (See MPEP 2114). Note that IBM clearly illustrates that each of the transfer gates is coupled to the input of one of the CMOS inverters that follow the transfer gate. Note that Q1 and Q4 forms part of an enable sircuit fo the oscillator. When "IN" is "low" the oscillator will oscillate i.e. Q2 and Q3 will form an inverter delay element. (See page 288 of IBM.) IBM is silent on showing of the structure that produces the two control signals that control the transfer gate transistors. Claim 4 recites that the first and second control signals both have two levels. Clearly these control signals of IBM each have at least two levels which is all that is required by the claim language. Claim 4 also sets forth that the claimed invention further includes "a control circuit in communication with [the] gates of said p-channel transistors with [the] gate of said n-channel transistors for shifting said first control signal between said two levels thereof and said second control signal between said two levels thereof". There must be a control circuit to provide the multiple control signal levels in IBM. IBM is merely silent on the details of such a circuit. Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have utilized a control circuit that can switch between the at least two levels of the first and second control signals in IBM because, as the IBM reference is silent on the exact control circuit used one of ordinary skill in the art would have been motivated to use any art-recognized equivalent control circuit such as the conventional control circuit that provides at least two signal levels for each of the control signals.

Claims 6, 7 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over IBM Technical Disclosure Bulletin vol. 33 No. 10A March 1991 (IBM) in view of Yunome 6,310,928 (Yunome).

Figure 1 and the relevant text of IBM discloses a voltage controller oscillator that has as part of its internal structure a ring oscillator composed of a feedback input terminal (The node that is directly connected to transistors Q13 and Q14 and line marked "OSCO".). Note that applicant calls the line 16 the

positive feedback loop in the specification and thus the "line", i.e. conductors connected between the two transistors Q13 and Q14, and the line marked "OSCO" forms the same "positive feedback loop" as per the specification. Also note the discussion below concerning the terminology "positive feedback loop" as per the plurality of delay stages. IBM also discloses a circuit output terminal "OSCO" that is clearly for generating an oscillator output signal and a "positive feedback loop" that is composed of a plurality of delay stages, i.e. like transistors Q2, Q7 and Q11 connected in cascade, and a transfer gate coupled to each of the plurality of delay stages. The transfer gates are composed of transistors like (Q5, Q6), (Q9, Q10), (Q13, Q14) wherein each of these transfer gates are composed of a pair of complementary transistors connected in parallel. The transfer gate transistors of the first conductivity type being controlled by a first control signal "PDEV" and the transfer gate transistors of the second conductivity type being controlled by a second control signal "NDEV". There are an odd number of delaying inverter stages like (Q7 and Q8) and (Q2 and Q3) clearly shown by IBM. These inverter stages are CMOS as is clearly illustrated in IBM. The claims recite the functional language "wherein said ring oscillator is operable during a first mode when said p-channel transistors are ON and said n-channel transistors are OFF, during a second mode when said p-channel transistors are OFF and said n-channel transistors are ON, and during a third mode when said p-channel and n-channel transistors are both ON". IBM recognizes that by changing the voltage of the two control signals that control the transfer gates that the time constant can be changed. Because the claim(s) do not recite a control signal source, the IBM reference has all of the claimed structure. Also the ring oscillator structure itself is clearly capable of providing for the functional language as recited above. This still results in the changing of the time constants as recognized by IBM. Thus IBM is fully capable of performing the recited function, (See MPEP 2114). Note that IBM clearly illustrates that each of the transfer gates is coupled to the input of one of the CMOS inverters that follow the transfer gate. Note that Q1 and Q4 forms part of an enable sircuit fo the oscillator. When "IN" is "low" the oscillator will oscillate i.e. Q2 and Q3 will form an inverter delay element. (See page 288 of IBM.) IBM is silent on showing of the structure that produces the two control signals that control the transfer gate transistors. Claim 4 recites that the first and second control signals both have two levels. Clearly these control signals of IBM each have at least two levels which is all that is required by the claim language. Claim 4 which claim 9 depends also sets forth that the claimed invention further includes "a control circuit in communication with [the] gates of said p-channel transistors with [the] gate of said n-channel transistors for shifting said first control signal between said two levels thereof and said second control signal between said two levels thereof". There must be a control circuit to provide the multiple control signal levels in IBM. IBM is merely silent on the details of

such a circuit. Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have utilized a control circuit that can switch between the at least two levels of the first and second control signals in IBM because, as the IBM reference is silent on the exact control circuit used one of ordinary skill in the art would have been motivated to use any art-recognized equivalent control circuit such as the conventional control circuit that provides at least two signal levels for each of the control signals.

Claims like claim 9 recite the additional structure of a "divider in communication with said circuit output terminal and operable to receive said oscillator output signal". Note that IBM is clearly a component of a larger system.

Figure 5 and the relevant text of Yunome describe one basis use for ring oscillator, namely the use in a phase locked loop.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have use the ring oscillator of IBM in a phase locked loop that has a divider connected to the output of the ring oscillator because, as the IBM reference is silent on the exact use of the ring oscillator component one of ordinary skill in the art would have been motivated to use the component in any art-recognized system that employs conventional ring oscillators such as the conventional phase locked loop that employs a ring oscillator whose output is connected to a divider such as the conventional phase locked loop arrangement of Yunome.

Claims 11, 12 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over IBM Technical Disclosure Bulletin vol. 33 No. 10A March 1991 (IBM) in view of Horn "Basic Electronics Theory" page 336 (Horn).

Figure 1 and the relevant text of IBM discloses a voltage controller oscillator that has as part of its internal structure a ring oscillator composed of a feedback input terminal (The node that is directly connected to transistors Q13 and Q14 and line marked "OSCO".). Note that applicant calls the line 16 the positive feedback loop in the specification and thus the "line", i.e. conductors connected between the two transistors Q13 and Q14, and the line marked "OSCO" forms the same "positive feedback loop" as per the specification. Also note the discussion below concerning the terminology "positive feedback loop" as per the plurality of delay stages. IBM also discloses a circuit output terminal "OSCO" that is clearly for generating an oscillator output signal and a "positive feedback loop" that is composed of a plurality of delay stages, i.e. like transistors Q2, Q7 and Q11 connected in cascade, and a transfer gate coupled to each of the plurality of delay stages. The transfer gates are composed of transistors like (Q5, Q6), (Q9, Q10), (Q13, Q14) wherein each of these transfer gates are composed of a pair of complementary

transistors connected in parallel. The transfer gate transistors of the first conductivity type being controlled by a first control signal "PDEV" and the transfer gate transistors of the second conductivity type being controlled by a second control signal "NDEV". There are an odd number of delaying inverter stages like (Q7 and Q8) and (Q2 and Q3) clearly shown by IBM. These inverter stages are CMOS as is clearly illustrated in IBM. The claims recite the functional language "wherein said ring oscillator is operable during a first mode when said p-channel transistors are ON and said n-channel transistors are OFF, during a second mode when said p-channel transistors are OFF and said n-channel transistors are ON, and during a third mode when said p-channel and n-channel transistors are both ON". IBM recognizes that by changing the voltage of the two control signals that control the transfer gates that the time constant can be changed. Because the claim(s) do not recite a control signal source, the IBM reference has all of the claimed structure. Also the ring oscillator structure itself is clearly capable of providing for the functional language as recited above. This still results in the changing of the time constants as recognized by IBM. Thus IBM is fully capable of performing the recited function, (See MPEP 2114). Note that IBM clearly illustrates that each of the transfer gates is coupled to the input of one of the CMOS inverters that follow the transfer gate. Note that Q1 and Q4 forms part of an enable sircuit fo the oscillator. When "IN" is "low" the oscillator will oscillate i.e. Q2 and Q3 will form an inverter delay element. (See page 288 of IBM.) IBM is silent on the integration of the circuit.

Horn discloses that it is advantageous to integrate a circuit so as to significantly reduce the size of the circuit and usually the cost.

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to integrate the circuit of IBM so as to significantly reduce the size of the circuit as taught by Horn.

Claim 14 recites that the first and second control signals both have two levels. Clearly these control signals of IBM each have at least two levels which is all that is required by the claim language. Claim 14 also sets forth that the claimed invention further includes "a control circuit in communication with [the] gates of said p-channel transistors with [the] gate of said n-channel transistors for shifting said first control signal between said two levels thereof and said second control signal between said two levels thereof". There must be a control circuit to provide the multiple control signal levels in IBM. IBM is merely silent on the details of such a circuit. Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have utilized a control circuit that can switch between the at least two levels of the first and second control signals in IBM because, as the IBM reference is silent on the exact control circuit used one of ordinary skill in the art would have been motivated to use

any art-recognized equivalent control circuit such as the conventional control circuit that provides at least two signal levels for each of the control signals.

Claims 8 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Technical Disclosure Bulletin vol. 33 No. 10A March 1991 (IBM) and Taito et al. 6,781,431 (Taito) as applied to claims 3, 5 and 22 above, and further in view of Yunome 6,310,928 (Yunome).

Claims like claims 8 and 10 recite the additional structure of a "divider in communication with said circuit output terminal and operable to receive said oscillator output signal". Note that IBM is clearly a component of a larger system.

Figure 5 and the relevant text of Yunome describe one basis use for ring oscillator, namely the use in a phase locked loop.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have use the ring oscillator of IBM in a phase locked loop that has a divider connected to the output of the ring oscillator because, as the IBM reference is silent on the exact use of the ring oscillator component one of ordinary skill in the art would have been motivated to use the component in any art-recognized system that employs conventional ring oscillators such as the conventional phase locked loop that employs a ring oscillator whose output is connected to a divider such as the conventional phase locked loop arrangement of Yunome.

Claims 13 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over IBM Technical Disclosure Bulletin vol. 33, No. 10A March 1991 (IBM) and Horn as applied to claims 11, 12 and 14 above, and further in view of Taito et al. 6,781,431 (Taito).

IBM is silent on showing of the structure that produces the two control signals that control the transfer gate transistors. Claim 15 recites that the first and second control signals both have two levels. Clearly these control signals of IBM each have at least two levels which is all that is required by the claim language. Claim 15 also sets forth that the claimed invention further includes "a control circuit in communication with [the] gates of said p-channel transistors with [the] gate of said n-channel transistors for shifting said first control signal between said two levels thereof and said second control signal between said two levels thereof". There must be a control circuit to provide the multiple control signal levels in IBM. IBM is merely silent on the details of such a circuit. Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have utilized a control circuit that can switch between the at least two levels of the first and second control signals in IBM because, as the IBM reference is silent on the exact control circuit used one of ordinary skill in the art would have been motivated to use any art-recognized equivalent control circuit such as the conventional

control circuit that provides at least two signal levels for each of the control signals. IBM is silent on the use of a NAND gate in place of one of the delay elements.

Figure 12 of Taito discloses the use of a NAND gate use in place of one of the delay elements in a ring oscillator so as to add the function of enablement/disablement and that this is an art recognized equivalent way to enable or disable a ring oscillator.

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to have replace on the delay/or element (Q1-Q4) of IBM with a NAND gate given that the NAND structure of Taito is an art recognized equivalent way to enable or disable a ring oscillator as compared to other conventional enable/disable circuits and so as to allow for an enable signal to control the enablement of the ring oscillator as taught by Taito.

Claims 16, 17 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Technical Disclosure Bulletin vol. 33 No. 10A March 1991 (IBM) in view of Horn "Basic Electronics Theory" page 336 (Horn) as applied to claims 11, 12 and 14 above, and further in view of Yunome 6,310,928 (Yunome).

Claims like claim 19 recite the additional structure of a "divider in communication with said circuit output terminal and operable to receive said oscillator output signal". Note that IBM is clearly a component of a larger system.

Figure 5 and the relevant text of Yunome describe one basis use for ring oscillator, namely the use in a phase locked loop.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have use the ring oscillator of IBM in a phase locked loop that has a divider connected to the output of the ring oscillator because, as the IBM reference is silent on the exact use of the ring oscillator component one of ordinary skill in the art would have been motivated to use the component in any art-recognized system that employs conventional ring oscillators such as the conventional phase locked loop that employs a ring oscillator whose output is connected to a divider such as the conventional phase locked loop arrangement of Yunome.

Claims 18 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Technical Disclosure Bulletin vol. 33 No. 10A March 1991 (IBM), Horn "Basic Electronics Theory" page 336 (Horn) and Taito as applied to claims 13 and 15 above, and further in view of Yunome 6,310,928 (Yunome).

Claims like claims 18 and 20 recite the additional structure of a "divider in communication with said circuit output terminal and operable to receive said oscillator output signal". Note that IBM is clearly a component of a larger system.

Figure 5 and the relevant text of Yunome describe one basis use for ring oscillator, namely the use in a phase locked loop.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have use the ring oscillator of IBM in a phase locked loop that has a divider connected to the output of the ring oscillator because, as the IBM reference is silent on the exact use of the ring oscillator component one of ordinary skill in the art would have been motivated to use the component in any art-recognized system that employs conventional ring oscillators such as the conventional phase locked loop that employs a ring oscillator whose output is connected to a divider such as the conventional phase locked loop arrangement of Yunome.

Allowable Subject Matter

Claims 23-30 are allowed.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael B. Shingleton whose telephone number is (571)272-1770. The examiner can normally be reached on Tues-Fri from 8:30 to 4:30. The examiner can also be reached on alternate Fridays. The examiner normally has second Mondays of the bi-week off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal, can be reached on (571)272-1769. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MBS
February 9, 2005

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